Department of Electrical Engineering
Response to Draft ABET Findings

Program Weaknesses

Criterion 2. Program Educational Objectives Criterion 2 states that the program must have "a process based on the needs of the program's various constituencies in which the objectives are determined and periodically evaluated." While a process exists, it is not clear that this process is clearly tied to feedback from the program's defined constituencies or what the time period is for re-evaluation of these objectives. Some objectives appear difficult to measure and some are similar to outcomes. Criterion 2 states that the program must have "a process of ongoing evaluation of the extent to which these objectives are attained, the result of which shall be used to develop and improve the program outcomes so that graduates are better prepared to attain the objectives." While evaluation has been done, it is not yet clear that this is an ongoing process and that the loop is being closed to use the evaluation results in program improvement.

Reply:

This Draft Finding for Criterion 2 identifies four areas where further clarification is required: (a) the role of feedback from the program's constituencies; (b) the time period for re-evaluation of the objectives; (c) the measurability of objectives and the similarity of objectives to outcomes; and (d) evidence that evaluation is an ongoing process and that the loop is being closed. We take these in turn below.

(a) Role of feedback from constituencies in the process of establishing Program Educational Objectives.

The Self-Study identified four constituencies: faculty, students, alumni, and industry/employers. It identified several mechanisms for collecting input from these constituencies, including input from our annual Board of Advisors meeting (board survey, board member commentary, board member direct review of PEOs), input from the Undergraduate Committee, qualitative and quantitative data collected from students (student performance in individual courses, end-of-course evaluations, EE 175 evaluation forms, senior exit survey), alumni surveys, and feedback forms from employers about intern performance.

All of the instruments described in the Self-Study and demonstrated at the site visit have been regularly applied through proper data collection strategies. We have a process in place for systematically collecting, evaluating, and responding to the data that we collect. As we point out below, we can demonstrate evidence that feedback from our constituencies is being used to make changes in our Objectives and in our Outcomes through our curriculum.

(b) The time period for re-evaluation of the objectives

As we noted in the response above, the success of these Objectives can only be measured properly several years after graduation. We obtain inputs at these intervals:

Faculty: (1) throughout the academic year when a problem or opportunity is identified, (2) annually when the entire faculty meets to review curricular changes.

Alumni: Annually, between three and five years after the bachelor's degree, through the College-wide alumni survey.

Industry/employers: (1) annually, at the department Board of Advisors meeting, (2) annually at the College Council of Advisors meeting, (3) periodically at the end of internships when they return survey

forms about student performance.

(c) Measurability of objectives and the similarity of objectives to outcomes

Section B.2.3 of the Self-Study contains a description of quantitative data sources that contribute to our evaluation of attainment of Program Educational Objectives. In 2006, we added a new instrument, a College-wide alumni survey, designed to provide more quantitative information on the achievement of Objectives. Figure 9 and Table 6 of the Self-Study showed quantitative information from our alumni regarding achievement of Objectives. The College-wide alumni survey instrument was available for inspection during the site visit, and a selection of relevant questions and responses is shown in Table 8 of the self-study. This is administered by the Office of the Dean to all College alumni between three and five years after completion of the bachelor's degree.

We proposed new PEOs, the board of advisors made some modifications, and we implemented the version that our board recommended. Here is what the self-study says: "Thus, the ABET committee, in consultations with the Chair and Undergraduate Committee, reformulated the EE PEO by revising the statements to make them more general and measurable. The proposed new PEO were presented to our BOA on May 12, 2006, revised based on BOA feedback, and approved by the EE faculty on May 17, 2006. The resulting improved PEO are shown above in section B.2.1." While the process was correct, the result was a set of PEOs some of which are difficult to quantitatively measure and some of which are similar to outcomes.

Therefore, in consultation with our constituencies, we are developing revised PEOs for Electrical Engineering and will have them in place during the spring quarter of 2007. These PEOs concisely summarize the two objectives of the undergraduate program, preparing students for success in graduate school and in industry. Furthermore, the examples are quantitatively measurable. The wording for the PEOs is as follows:

Graduates of UCR's BS degree program in Electrical Engineering will be capable of achieving:
success in post-graduation studies as evidenced by:

- satisfaction with the decision to further their education
- advanced degrees earned
- professional visibility (e.g., publications, presentations, patents, inventions, awards)
- international activities (e.g., participation in international conferences, collaborative research, employment abroad)

success in their chosen profession as evidenced by:

- career satisfaction
- promotions/raises
- professional visibility (e.g., publications, presentations, patents, inventions, awards)
- entrepreneurial activities
- international activities (e.g., participation in international conferences, collaborative research, employment abroad)

The Electrical Engineering faculty initiated this new set of PEOs. We have solicited comments from the following constituencies: members of the student chapter of IEEE, members of the Undergraduate Leadership Council, members of EE's board of advisors, and all alumni of the program. This feedback will be discussed at the May 2007 meeting of the advisory board for EE. All feedback, including the minutes of those meetings, will then be considered by the accreditation committee for EE. The committee will draft a final version of the PEOs, which will be voted on by the EE faculty. That final version will be

published on the program's web site in May 2007 and in the next edition of UCR's General Catalog.

(d) Evidence that evaluation is an ongoing process and that the loop is being closed.

Evidence of "closing the loop" is in the form of changes to the curriculum designed to put our students on the path to achieving the program educational objectives early in their careers or during graduate study.

Examples of changes that we have made in response to the feedback we have received include the following:

EE10 was implemented as part of our effort to retain entering EE students. As described in Sec. B.1.1, pp. 3-4 of the EE Self-Study, COE loses 40% of its students during their first 2 years. Exit surveys of graduating seniors indicated that lack of engagement with the College in the early years was a problem. EE10 was designed to give freshmen an immediate contact with and understanding of EE using everyday technology examples. EE10 provides students with an early positive engineering experience and interaction with departmental faculty.

Initiating EE faculty advising and mentoring was also part of our response to the retention problem. Freshmen immediately come into contact with EE professors.

As a result of input from advisory boards, a course on technical communications (Engineering 180) has been established and adopted as a requirement for Electrical Engineering, thereby enhancing the degree to which graduates will have achieved outcome (g) and the degree to which outcome (g) will be assessed. Faculty were unanimously in favor of adding ENGR 180 as a technical elective on 11/30/2005, and voted to reduce the overall technical elective requirement to accommodate this course on 3/10/2006.

In response to feedback from undergraduate students and the board of advisors, the EE technical electives were grouped into specialization areas within the EE program, and a faculty advisor was assigned for each area to help students with their course selection.

As a result of concerns raised on the exit surveys of seniors, the College of Engineering established a position of Career Development and Placement Officer to assist graduating students and alumni in pursuit of their careers and the degree to which they achieve the PEOs.

Finally, as result (in part) of dissatisfaction registered in exit surveys throughout the campus, UCR appointed a Task Force on Student Success, chaired by Reza Abbaschian, Dean of the Bourns College of Engineering, who made use of the College's feedback and assessment tools in leading this group. The Task Force recommended numerous changes to the freshman experience, student advising, student surveys, and University investments in support of teaching and learning. At least two of the recommended changes were pioneered in Engineering: the development of "learning communities" in which students take several introductory-level courses together, and the establishment of some tutoring and mentoring services in campus dormitories.

Criterion 3. Program Outcomes and Assessment Criterion 3 requires "… an assessment process, with documented results, that demonstrates … program outcomes are being measured and indicates the degree to which the outcomes are achieved." While some assessment has been implemented, it does not appear that all outcomes are sufficiently measured and that achievement of all outcomes is being demonstrated. Sufficient evidence was not provided for the following outcomes: "b" an ability to design and conduct experiments, "d" an ability to function on multi-disciplinary teams, "f" an understanding of professional and ethical responsibility, "h" the broad education necessary to understand the impact of engineering

solutions in a global, economic, environmental, and societal context, "j" a knowledge of contemporary issues.

Reply

While items b, f, h, and j have been part of the material taught in the two quarter Senior Design project, EE175a,b, the demonstration of these outcomes was not well documented. The syllabus of EE175a,b has been rewritten so that these outcomes are explicitly included with corresponding assignments that will be documented and used to measure the students' performance in obtaining these outcomes. The revised syllabus explicitly showing the assignments associated with these outcomes is shown in App. A. The final report template with required sections related to these areas is shown in Appendix B. Starting this Winter and Spring quarters, items b, f, h, and j will be documented for all EE students in either the EE175 final report, exam, or essay assignment. These instruments will be used to measure the program outcomes.

Item d, an ability to function on multi-disciplinary teams, is being addressed in the two cross-listed courses EE/CSE 120A/B. All Electrical Engineering, Computer Engineering, and Computer Science students are required to take this sequence of courses. It was decided that for both EE/CSE 120A and 120B, lab partners will be rotated weekly until every student in the class has worked on one interdisciplinary team. The lab assignments from the interdisciplinary teams will be an instrument for demonstrating and measuring the students' ability to function on interdisciplinary teams. The revised catalog text for the courses is shown in Appendix C, and the revised syllabus for 120A is shown in Appendix D.

Criterion 4. Professional Component Criterion 4 states, "Students must be prepared for engineering practice through the curriculum culminating in a major design experience based on the knowledge and skills acquired in earlier course work and incorporating appropriate engineering standards and multiple realistic constraints." While the senior design projects in EE175 are of excellent quality, inspection of a sample of reports and oral presentations did not provide sufficient evidence to demonstrate that all projects incorporate engineering standards and realistic constraints.

Reply

While these were included, they were not adequately documented. To ensure proper documentation, the course syllabus for EE175a/b (Appendix A) has been revised to include these items in the "Detailed Design Specification." Realistic constraints and industry standards are required sections (Sections 3.2 and 3.4, respectively) of the EE175AB final report template shown in Appendix B.

Criterion 4 also states, "The professional component must include … one and one-half years of engineering topics, consisting of engineering sciences and engineering design appropriate to the student's field of study." The program currently contains 66 quarter hours of electrical engineering topics, plus 20 hours of technical electives. Depending on how these electives are selected, it is possible for students to take 16 hours of computer science, which could lead to graduation without the 72 hours of electrical engineering topics required by this criterion.

Reply

The description of the choice of EE electives in the UCR catalog has been modified to read: "The choice of technical electives must ensure that the upper division requirements include at least one coherent sequence of at least three (3) electrical engineering courses to ensure depth in one area of electrical engineering. Example course sequences are available through the Student Affairs Office in the College of Engineering or http://www.engr.ucr.edu /studentaffairs/."

This ensures 78 quarter hours of electrical engineering topics.

Criterion 8. Program Criteria The electrical engineering program criteria state, "The program must demonstrate that graduates have: knowledge of probability and statistics, including applications appropriate to the program name and objectives …." The program has a required course in probability and statistics taught by the mathematics and statistics faculty, but does not demonstrate applications appropriate to electrical engineering theory and practice.

Reply

The EE faculty decided that the best way to address this was to propose a new EE course, EE114 Probability, Random Variables, and Random Processes in Electrical Engineering, to replace the required course Stat 155. The new course includes applications specific to EE as shown in the syllabus of the course proposal included in Appendix E. The course will be in the 2007 – 2008 catalog and offered in the Spring of 2008.

Criterion 8 also states, "The structure of the curriculum must provide both breadth and depth across the range of engineering topics implied by the title of the program." While the curriculum insures that all students achieve adequate depth, the rules governing the selection of electives make it possible for a student to graduate by taking only introductory courses in multiple areas thus not achieving depth in any area.

Reply

The description of the choice of EE electives in the UCR catalog has been modified to read, "The choice of technical electives must ensure that the upper division requirements include at least one coherent sequence of at least three (3) electrical engineering courses to ensure depth in one area of electrical engineering. Example course sequences are available through the Student Affairs Office in the College of Engineering or http://www.engr.ucr.edu /studentaffairs/."

The student affairs officers in the Student Affairs office ensure that the coherent sequence is chosen from one of the 4 focus areas described in Appendix F.

Appendix A

Bourns College of Engineering, University of California, Riverside

EE-175: Senior Design Project

Winter and Spring 2007

Class

Lecture: Mondays 10:10 a.m. - 11:00 a.m. STAT B650
Lab: to be arranged with section professor

Instructors:

Professor Amit Roy Chowdhury	amitrc@ee.ucr.edu	EBU-II 322	827-7886
Professor Yingbo Hua	yhua@ee.ucr.edu	EBU-II 432	827-2853
Professor Sakhrat Khizroev	khizroev@ee.ucr.edu	EBU-II 424	827-5816
Professor Ping Liang	liang@ee.ucr.edu	EBU-II 323	827-2261
Professor Mihri Ozkan	mihri@ee.ucr.edu	EBU-II 436	827-2900
Professor Sheldon Tan	stan@ee.ucr.edu	EBU-II 424	827-5143

Prerequisites

Senior standing in Electrical Engineering.

Objectives

The Senior Design Project is the culmination of course work in the bachelor's degree program in electrical engineering or computer engineering. In this comprehensive two-quarter course, students are expected to apply the concepts and theories of electrical engineering or computer engineering to an engineering project. Detailed written reports, working demonstration, poster and oral presentations are required.

Credits and Hours

Eight quarter units of engineering design credit will be granted for the completed project and other required components listed here. It is expected that approximately twelve hours of laboratory (or field) work will be required weekly for satisfactory completion of the project. The design value of these units has been accounted for in the total number of required science and design units necessary for graduation.

Weekly Class Meetings

The entire class of EE 175A and EE 175B will meet once each week for one hour. These meetings are intended to provide instruction in topics common to all design projects (engineering economics, ethics, etc.). They may include brief presentations by each team, aimed at improving technical presentation skills. Lectures will be provided by the instructors and some outside contacts. These meetings are mandatory and are for your benefit (10% of grade). In addition, it is

expected that each project team meet with their faculty supervisor on a weekly basis to report and discuss the progress of the project.

Project Participants

Projects will be completed in small teams with shared responsibility. If the team option is elected, each student will be held responsible for a distinct component of the total team effort. Team projects will be sufficiently more complex than individual projects so as to allow for an appropriate workload for all team members.

Project Elements

The senior design projects will include proposal and report writing, experiment design, hardware and software design, test plan and test, broad impact and ethical issues, among other things. Remember that this is a design course and students must define a ***design*** project, not a research, nor an evaluation or fabrication project. It is a balanced approach to encompass many of the elements stated above.

Each design project must include the following components:

1. **A Clear Technical Design Objective and the Project Contract** (Contract due 1/22/07): Each group must identify a design project in the first two weeks of the Winter quarter, and should have good estimated answers to the following questions and obtain the endorsement of the section professor:
   - Is the objective achievable within two quarters?
   - Does the group have the expertise to complete the design, prototype, and testing?
   - Does the group have access to the financing for the prototype?
   - Does the group have access to the required test equipment?
   - Is this a design problem (not research, nor fabrication)?
   - Is the project significant enough to be worthy of eight credits (12 hours/week/person)?

2. **Experiment Design and Feasibility Study** (Due in week 5 to 6 of the Winter quarter, 5% of final grade)**:** Each group must write an Experiment Design document, which describes its design of experiments to evaluate the feasibility of its project ideas, alternatives, trade-offs and realistic engineering constraints. These experiments must then be carried out and experimental results are to be analyzed to prove the feasibility of your project idea and select the best solution to be further developed in the design project. The experimental data, the quantitative analysis of the data, and the conclusion are to be presented in a Feasibility Study Report.

3. **A Detailed Design Specification** (Due in week 7 to 9 in the Fall quarter, 10% of final grade): Describes the functions and quantitatively measurable design objectives, design methods, hardware and software architecture and interfaces, user interface, realistic constraints in terms of time, cost, safety, reliability, social impact, ethics, etc. It must also list and consider the industry standards related to your project, including hardware, protocols, software and tools (e.g., 802.11, RS232, USB, PCI, 3G, API, device drivers, VHDL).

4. **Test Plan** (Due in week 8 to 9 of the Fall quarter, 5% of final grade)**:** A detailed description of your design of experiments to test and measure whether the final product and each of its

components meet the design specifications, and, if not, to test and measure the errors and deviations from specifications.

5. **Global, economic, environmental and societal impact** (Due 2/12/07, 2.5% of final grade): Each student must write an essay (800 or more words) providing an analysis of the potential global, economic, societal, and environmental impact of the project. You do not need to address every aspect, just focus on a couple of aspects that are related to your project. For example, if your project is made into a product, how will it improve quality of life, affect the environment, enhance entertainment, education, globalization etc.? Are there any ethical or political debates, laws and regulations that are related to your project?

6. **Contemporary Engineering issues** (Due 2/26/07, 2.5% of final grade) Provide in essay form a description of the contemporary engineering issues related to the project. Potential contemporary engineering issues related to your project are new technologies, new industry standards, new design methods, new materials, new trends in manufacturing, etc.

7. **Detailed Quantitative Design and Prototype** (To be completed before week 9 of the Spring Quarter) Each component of the selected solution and the overall system should be designed and implemented. In most cases, it is necessary to construct a system prototype (or component prototype).

8. **Test Report** (Due week 10 of the Spring quarter, 5% of final grade): Carry out the Test Plan you developed to MISSING WORD? how well your final design meet the specifications under the defined constraints, and present the results in this report.

9. **Poster and Final Presentation** (Due week 10 of the Spring quarter, 15% of final grade): Each group must prepare a poster and a Power Point presentation, and present the final design to faculty and other students.

10. **Working Demo and Final Report** (Due 6/8/2007 before 5pm, 40% of final grade): The final report must include all the required sections and appendices in a template file to be posted on the iLearn website for the course. A working demo of the completed design is critical, it is a convincing evidence that you design is completed and works. The demo should show whether and how design specifications are met.

Grading

In addition to the 9 deliverables listed above, each project will also be graded on the following:

1. **Laboratory Notebook, Weekly Reports and Lecture Attendance—**The student teams will need to maintain a laboratory notebook for the duration of their projects and submit written weekly reports. This notebook and reports will be inspected at weekly meetings and graded for content. Attendance of the lectures is mandatory. Everyone must sign in at each lecture. (This portion accounts for 10% of grade)
2. **Ethics Exam**: 5% of the final grade

Grading will be determined by all of the section professors conferring on each project and student. Please note that grades are assigned to an individual, not to a project.

Project Topics

Projects will be carried out in four different sections corresponding to the main electrical engineering areas taught at UCR. Each section will have a "section professor" (i.e., faculty supervisor) as designated below. Possible project topics are obtained from the section professor. In addition, joint projects with the mechanical engineering department are possible.

Electrical Engineering Area	Section Professor	Topics
Nano-Materials, Devices and Circuits (NMDC)	Mihri Ozkan and Sakhrat Khizroev	***Solarium Environment and Solar Cell Development*—**Students will build an environmental test chamber (i.e., Solarium) that is capable of simulated sunlight at different intensities. The students will then fabricate organic solar cells and subsequently characterize these designs in the environmental test chamber.
Intelligent Systems (IS)	Ping Liang	***Embedded systems, video processing*—**Projects may include video processing, wireless networking and embedded systems. Students may choose their own project subject to the approval of the instructor.
Controls and Robotics (CR) (& Sensing)	Amit Roy Chowdhury	***Image Processing*—**Other projects include face recognition, video based digital map design, and the synthesis of human activities using learned dynamical models.
Communications and Signal Processing (CSP)	Yingbo Hua and Sheldon Tan	***Ad Hoc Communication Networks*—**Projects include building and testing a network of three or more wireless nodes that can communicate with each other. Students will search and buy commercially available wireless transceivers, and then design, develop, and implement communication protocols into the network. Students will demonstrate that their network can indeed perform communications among its nodes without assistance from any established base station. ***Communication electronic design*—**Projects include designing optical wavelength locking sub-system(s) for semiconductor DFB lasers; developing high-speed analog/digital electronics for a 10 Gb/s duobinary communications receiver; and designing an optical phase stabilization sub-system using fiber optics, analog electronics, and feedback principles. ***Signal Processing for VLSI*—**projects include designing signal-processing algorithms for a variety of VLSI systems.

Steps in Selecting a Project

Upon reviewing the topic areas, students should invoke the following steps to select a project, and sign the corresponding senior design contract (next page), in order to "officially" register for the course.

Step - 0: Prepare a brief academic resume, which describes your specific technical strengths and general background in less than two pages. It is very important that you make a case for yourself as to why you should be doing a specific project. This step is more or less like applying for a job, and therefore this resume is the first draft of your future resume that opens a door for you. Then follow one of the following Steps 1A to 1C, depending on your situation.

Step - 1A: Make an appointment to meet and talk to the section professors with whom you wish to work, and see whether they are willing to recommend you for their projects. At a minimum you should talk to two (preferably three) professors. Alternatively:

Step - 1B: If you have an industrial project in mind that meets the requirements stated above, then you still need to talk to an EE175 section professor. This professor must approve and supervise the project. Alternatively:

Step - 1C: If none of the above projects appeals to you, but you have your own ideas, then you must lobby for that idea with a section professor. This approach requires additional effort, but is doable if it is planned in advance.

Step - 2: Identify one or possibly two of your classmates who have similar interests and want to work with you on the same project and have gone through the same steps as you did. Discuss the project among team members and achieve a consistent project idea.

Step - 3: Make a brief written proposal to the section professor that includes your resume, your classmate(s) resume(s) if applicable, the title of the project, and a brief description. Also have at least two more project titles in this proposal as your second and third choices. Please note that every effort will be made to match you with your best choices, although in certain instances changes may be required. In that case you will be notified promptly.

Step – 4: Once the projects are orally approved by the section professors, each student team is to fill out a project contract available on the class web site. Be sure to fill out every section, sign it, and turn it in to your section professor.

Appendix A

Approximate Class Schedule

Date	Event	Lecturer	Lecture Content
1/8	Lecture 01	All	Introduction, course outline, preliminary issues, requirements and expectations
1/15	Lecture 02		Holiday, no class
1/22	Lecture 03	MO	Technical writing
1/29	Lecture 04	YH	Design methodologies and approaches; block diagrams, analyses of solutions, evaluation of feasibility
2/5	Lecture 05	AC	Experiment design, developing a test plan, collecting data, and evaluation
2/12	Lecture 06	SK	Introduction to the design process, specification process, laboratory notebooks, library techniques, literature and information search
2/19	Lecture 07		Holiday, no class
2/26	Lecture 08	SK	Project management: organization, teamwork, scheduling, budgeting, etc.
3/5	Lecture 09	MO	How to give oral presentations, preparing for the design review
3/12	Lecture 10	AC	Design constraints, industry standards
TBD	Design Review	All	Two parallel sessions
4/2	Lecture 11	DG	Printed circuit board design, layout, and fabrication
4/9	Lecture 12	ST	Contemporary engineering issues
4/16	Lecture 13	SK	Engineering ethics (exam required)
4/23	Lecture 14	PL	Intellectual properties
4/30	Lecture 15	ST	Career strategies, resumes
5/7	Lecture 16	PL	Engineering economics, marketing engineering products
5/14	Lecture 17	ST	Final testing requirements, test report, preparation for the final presentation
5/21	Lecture 18	PL	Entrepreneurial, venture capital and start-ups
5/28	Lecture 19	MO	Societal, environmental and cultural impact, international engineering projects
6/4	Final Presentations.	All	Poster required. Two parallel sessions

Lecturer code: **AC -** Amit Chowdhury, **DG** – Dan Giles, **YH** – Yingbo Hua, **SK** - Sakhrat Khizroev
PL – Ping Liang **MO** – Mihri Ozkan, **ST** – Sheldon Tan

Learning Objectives

- Ability to apply knowledge of mathematics, science, and engineering
- Ability to design and conduct experiments, as well as analyze and interpret data
- Ability to design a system, component, or process to meet desired needs
- Ability to function as effective teams
- Ability to identify, formulate, and solve engineering problems
- Understanding of professional and ethical responsibility
- Ability to communicate effectively
- Broad education necessary to understand the impact of engineering solutions in a global and societal context
- Recognition of the need for and an ability to engage in lifelong learning
- Knowledge of contemporary issues
- Ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

EE175AB Final Report Template

Revised Catalog text for EE 120A and EE 120B

EE 120A. Logic Design (5) Lecture, 3 hours; laboratory, 6 hours. Prerequisite(s): CS 061 with a grade of "C-" or better. Covers the design of digital systems. Topics include Boolean algebra; combinational and sequential logic design; design and use of arithmetic-logic units, carry-lookahead adders, multiplexors, decoders, comparators, multipliers, flip-flops, registers, and simple memories; state-machine design; and basic register-transfer level design. Interdisciplinary laboratories involve use of hardware description languages, synthesis tools, programmable logic, and significant hardware prototyping. Cross-listed with CS 120A.

EE 120B. Introduction to Embedded Systems (5) Lecture, 3 hours; laboratory, 6 hours. Prerequisite(s): CS 120A/EE 120A. Introduction to hardware and software design of digital computing systems embedded in electronic devices (such as digital cameras or portable video games). Topics include embedded processor programming, custom processor design, standard peripherals, memories, interfacing, and hardware/software tradeoffs. The interdisciplinary laboratory involves use of synthesis tools, programmable logic, and microcontrollers and development of working embedded systems. Cross-listed with CS 120B.

Appendix D

Department of Electrical Engineering
University of California – Riverside

EE 120A LOGIC DESIGN

(Prerequisite: CS 061)

Lecture:
Section 001: MWF 2:10 – 3:00 p.m., Boyce Hall 1471
Instructor: Dr. Vladimir Fonoberov

Web: http://www.faculty.ucr.edu/~vladimf/ & http://www.iLearn.ucr.edu/
Office Hours: MW 1:10 – 2:00 p.m., ENGR2 408

Labs:
Section 021: MT 6:10 – 9:00 p.m., ENGR2 125
TA: Lingfei Zhou (lzhou001@student.ucr.edu)

Section 022: RF 11:10 a.m. – 2:00 p.m., ENGR2 125
TAs: Ben Fellows (bfellows@ee.ucr.edu) & Zhuo Zhao (zhaozhuo@ee.ucr.edu)

Catalog Description:
Covers the design of digital systems. Topics include Boolean algebra; combinational and sequential logic design; design and use of arithmetic-logic units, carry-lookahead adders, multiplexors, decoders, comparators, multipliers, flip-flops, registers, and simple memories; state-machine design; and basic register-transfer level design. Laboratories involve use of hardware description languages, synthesis tools, programmable logic, and significant hardware prototyping.

Text:
"***Digital Design***" by Frank Vahid, John Wiley & Sons, 2006 (ISBN 0-471-46784-7)

Homework:
Four homework assignments will be given during the course. Solution of the homework problems will normally require reading the book, working on examples, and reviewing class material. Homework must be typed or very neatly written.

Quizzes:
Four 50-minute quizzes will be given during the course.

Labs:
Eight lab assignments and one lab exam will be given. Lab attendance is required for the full 3-hour lab. For the first part of the course, the Instructor and TAs will form interdisciplinary teams of two students, e.g. one EE student and one CS/CE student. New teams will be formed each week (for each lab assignment). Each lab report must show students' names and majors.

Midterm: February 9, 2007 (subject to change)
Final Exam: March 22, 2007; 8 – 11 a.m.

Grading:
- **Lecture component** (70 points)
  - 30 pts: Final
  - 20 pts: Midterm
  - 10 pts: Quizzes (4 @ 2.5 pts)

  - 10 pts: Homework (4 @ 2.5 pts)
- **Lab component** (30 points)
  - 24 pts: Lab assignments (8 @ 3 pts)
  - 6 pts: Lab practical exam

EE 114 Course proposal

Probability, Random Variables, and Random Processes in Electrical Engineering

Appendix F

EE Focus Areas

1. Controls and Robotics (CR)
EE132 Automatic Control
EE128 Data Acquisition and Process Control
EE141 Digital Signal Processing
EE144 Introduction to Robotics
EE146 Computer Vision
EE151 Introduction to Digital Control
EE152 Image Processing

2. Communications and Signal Processing (CSP)
EE141 Digital Signal Processing
EE117 Electromagnetics-II
EE128 Data Acquisition and Process Control
EE143 Multimedia Technologies and Programming
EE146 Computer Vision
EE150 Digital Communications
EE152 Image Processing
EE160 Fiber Optic Communication Systems.

3. Intelligent Systems (IS)
EE141 Digital Signal Processing
EE128 Data Acquisition and Process Control
EE140 Computer Visualization
EE143 Multimedia Technologies and Programming
EE146 Computer Vision
EE144 Introduction to Robotics
EE152 Image Processing

4. Nano Materials, Devices and Circuits (NMDC)
EE133 Solid-State Electronics
EE117 Electromagnetics-II
EE130 Engineering Quantum Computing
EE134 Digital Integrated Circuit Layout and Design
EE135 Analog Integrated Circuit Layout and Design
EE136 Semiconductor Device Processing Lab
EE141 Digital Signal Processing
EE160 Fiber Optic Communication Systems